SED1530 Series

DOT MATRIX LCD DRIVER-CONTROLLER

■ DESCRIPTION

The SED1530 Series are intelligent CMOS LCD controller-drivers with the ability to drive alphanumeric and graphic displays. The LSI communicates with a high-speed microprocessor, such as the Intel 80xx and 68xx family, through either a serial or 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (65 × 132 bits) and generates an LCD drive signal.

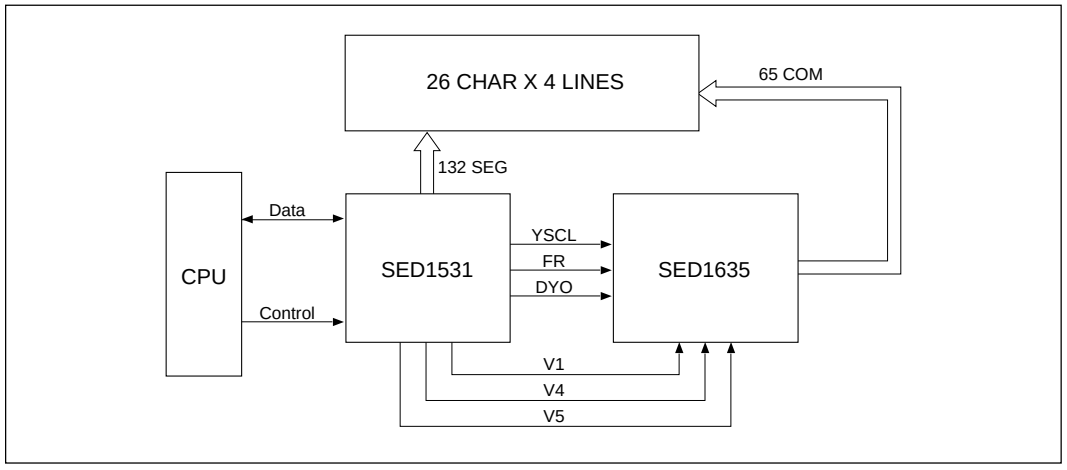
■ FEATURES

- Low-power CMOS technology
- Direct interface to both 80xx and 68xx MPU
- Support 8-bit parallel and serial interface
- On-chip display data RAM ..... 132 × 65 bits
- On-chip DC/DC converter for LCD voltage
- On-chip CR oscillator circuit
- Supports master/slave mode
- Voltage regulator, low-power voltage follower
- –.17%/°C temperature gradient
- 32-level contrast adjustment by software
- 2.4V to 6.0V supply voltage
- –4.5V to –16V LCD voltage
- Operating temperature ..... –40 to 85°C
- Low power consumption 80µA
- Package
  - TAB ..... T**
  - Al pad Die ..... D*A
  - Au bump Die ..... D*B

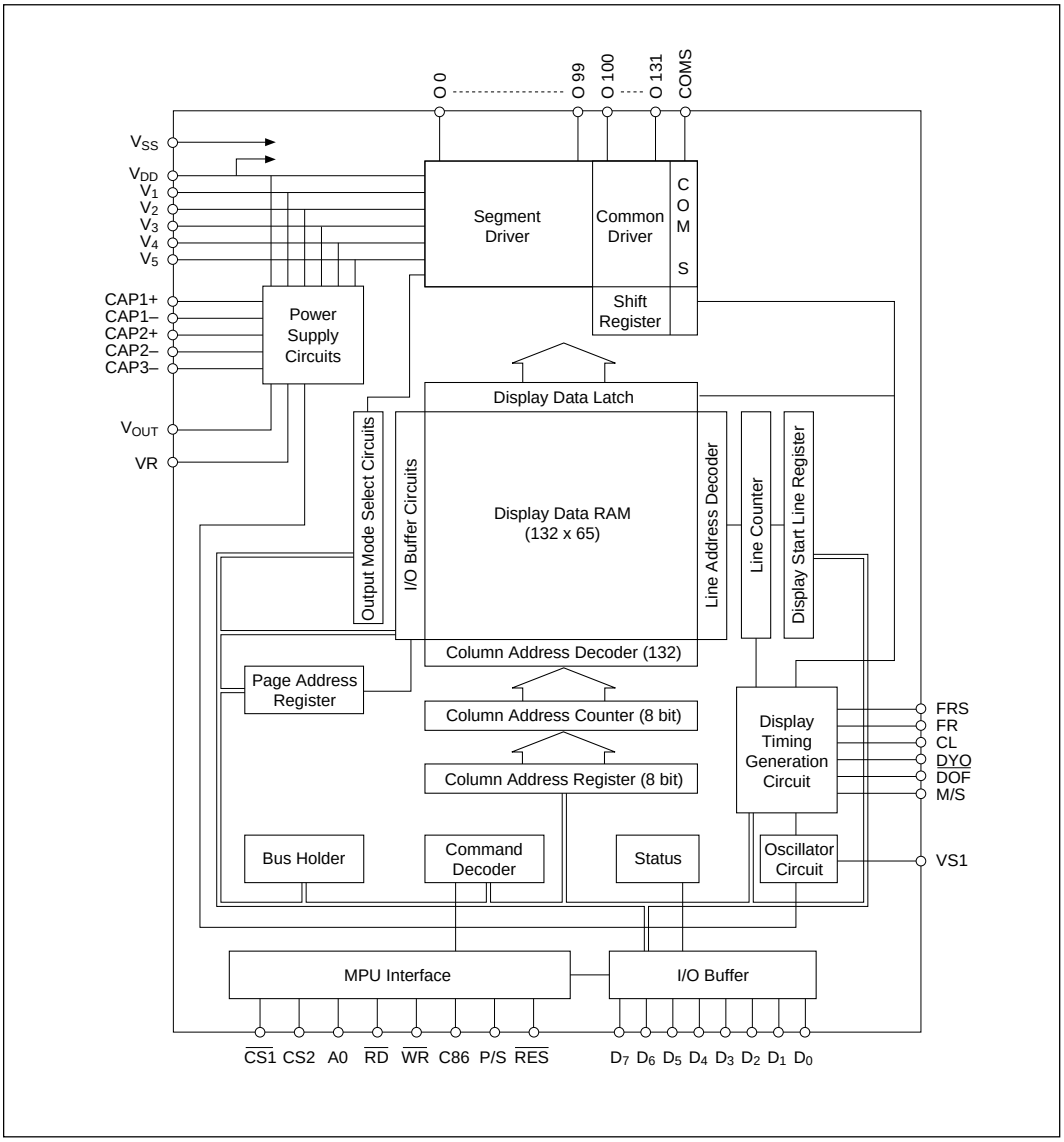
■ AVAILABLE MODELS

Name	Duty	LCD Bias	SEG Driver	COM Driver	Display Area	Remarks
SED1530D0*	1/33	1/5,1/6	100	33	33 × 100	COM single-side assignment
SED1530DA*	1/33	1/5,1/6	100	33	33 × 100	COM dual-side assignment
SED1531D0*	1/65	1/6,1/8	132	0	65 × 132	SED1635 is used for COM
SED1532D0*	1/65	1/6,1/8	100	33	65 × 200	COM single-side right assignment
SED1532DB*	1/65	1/6,1/8	100	33	65 × 200	COM single-side left assignment

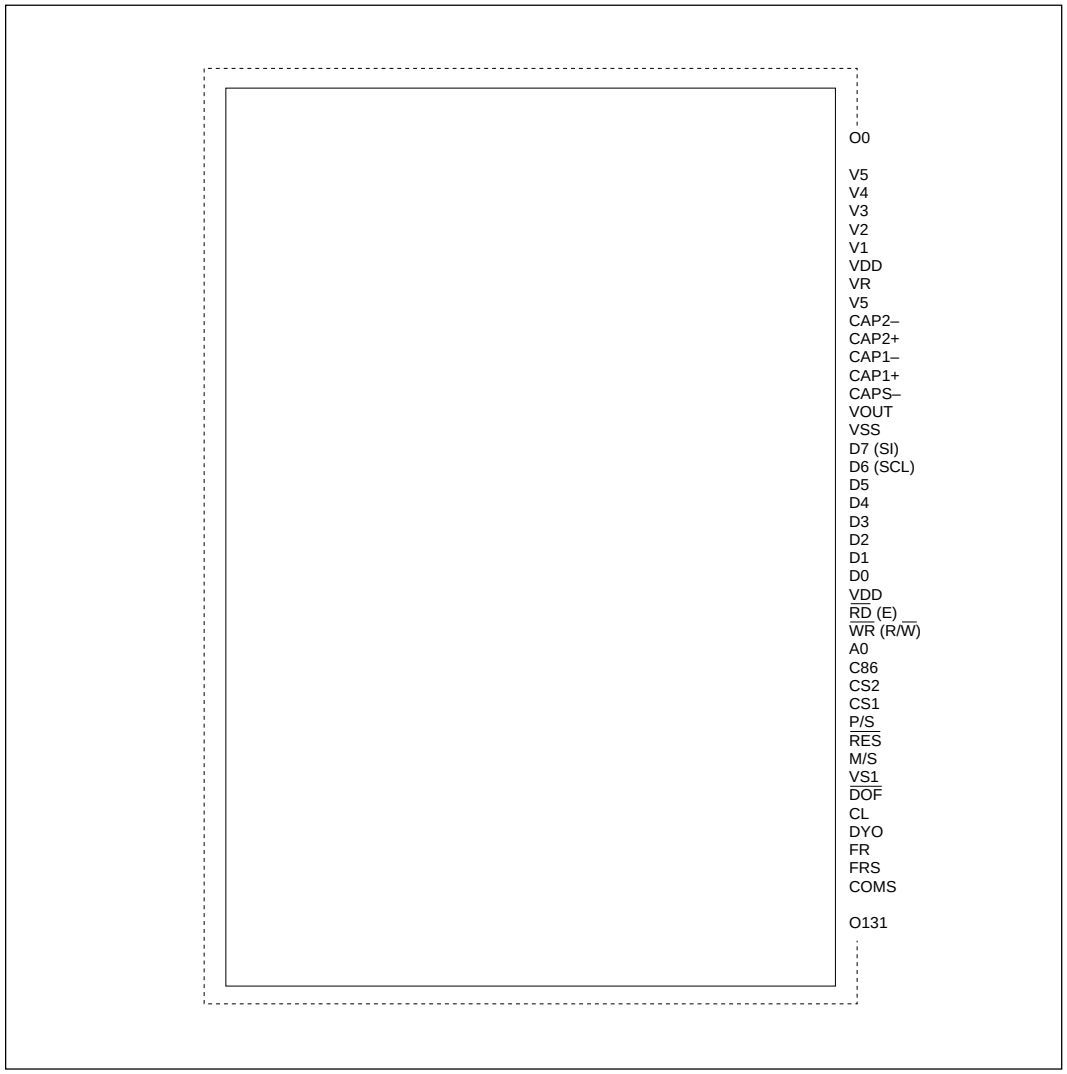
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PINOUT



■ PINOUT TABLE

Model	Output	O_0 to O_{15}	O_{15} to O_{31}	O_{32} ---------- O_{99}	O_{100} to O_{115}	O_{116} to O_{131}
SED1530*0*	0	SEG0 ---------- SEG99			COM0 ---------- 31	
	1				COM31 ---------- 0	
SED1530*A*	0	COM15 -- 0	SEG0 ---------- SEG99			COM16 31
	1	COM16 31				COM15 -- 0
SED1531*0*		SEG0 ---------- SEG131				
SED1532*0*	0	SEG99 ---------- SEG0				COM31 -- 0
	1					COM0 -- 31
SED1532*B*	0	COM0 -- 31	SEG0 ---------- SEG99			
	1	COM31 -- 0				

Note: * "0" and "1" indicate the mode of the D3 output mode select register.

■ PIN DESCRIPTION

● Power Signals

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>V_{DD}</td><td>Power</td><td>Connected to +5V power. Connected with MPU power supply V_{CC} pin.</td><td>2</td></tr>
<tr><td>V_{SS}</td><td>Power</td><td>0V, connected to system GND.</td><td>1</td></tr>
<tr><td>V1 ~ V5</td><td>Power</td><td>Multi-level power for LC driver. Transforms impedance using resistive voltage divider or op amps in order to apply the voltage determined for each LC cell. The voltage levels are based on V_{DD}, and must conform to the relationship below:
$V_{DD} \geq V0 \geq V2 \geq V3 \geq V4 \geq V5$
When the master operation power supply is ON, the internal power supply circuitry supplies the V1 ~ V4 voltages shown below. The voltage levels are selected using the LCD bias set command.
<table>
<tr><th></th><th>SED1530D0*</th><th>SED1530DA*, SED1531D0*, SED1532D**</th></tr>
<tr><td>V1</td><td>1/5 × V5 1/6 × V5</td><td>1/5 × V5 1/6 × V5</td></tr>
<tr><td>V2</td><td>2/5 × V5 2/6 × V5</td><td>2/5 × V5 2/6 × V5</td></tr>
<tr><td>V3</td><td>3/5 × V5 4/6 × V5</td><td>3/5 × V5 4/6 × V5</td></tr>
<tr><td>V4</td><td>4/5 × V5 5/6 × V5</td><td>4/5 × V5 5/6 × V5</td></tr>
</table>
</td><td>6</td></tr>
</table>

● LCD Power Circuit Pins

Pin	I/O	Function	Number of Pins
CAP1+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP1–.	1
CAP1–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
CAP2+	O	Voltage step-up capacitor, positive side connection pin. Connect the capacitor between this pin and CAP2–.	1
CAP2–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP2+.	1
CAP3–	O	Voltage step-up capacitor, negative side connection pin. Connect the capacitor between this pin and CAP1+.	1
V_{OUT}	O	Voltage step-up output pin. Connect the capacitor between this terminal and V_{SS}.	1
V_R	I	Voltage regulator pin. Use a resistive voltage divider to provide voltage between V_{DD} and V5.	1

- **System Bus Interface Signals**

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>D7 ~ D0
(SI)
(SCL)</td><td>I/O</td><td>8-bit bi-directional data bus, normally connected to a standard 8-bit or 16-bit MPU data bus.
When serial interface is selected:
D7: Serial Data Input Pin (SI)
D6: Serial Clock Input Pin (SCL)</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the LSB of the MPU address bus is connected to this pin to provide data/command selection:
0: D0 ~ D7 indicate display control data
1: D0 ~ D7 indicate display data</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Reset to initial settings by setting $\overline{RES}$ to “L”.
The reset operation is performed according to the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip Select input pins. Data I/O is enabled by the combination below:
<table><tr><td>Pin Name</td><td>$\overline{CS1}$</td><td>CS2</td></tr><tr><td>State</td><td>“L”</td><td>“H”</td></tr></table></td><td>2</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>* When connected to an 80-series MPU:
Active “L”
This pin is connected to the $\overline{RD}$ signal from the MPU. When this signal is “L” the SED1530 Series data bus is in output mode.
* When connected to a 68-series MPU:
Active “H”
This is the 68-series MPU enable clock input pin.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>I</td><td>* When connected to an 80-series MPU:
Active “L”
This pin is connected to the $\overline{WR}$ signal from the MPU. The data bus signals are retrieved at the rising edge of the $\overline{WR}$ signal.
* When connected to a 68-series MPU:
This is the read/write control signal input pin.
R/$\overline{W}$ = “H”: Read
R/$\overline{W}$ = “L”: Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface select pin:
C86 = “H”: the 68-series MPU interface
C86 = “L”: the 80-series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Serial data input/parallel data input selection pin:
<table><tr><td>P/S</td><td>Chip Select</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr><tr><td>“H”</td><td>$\overline{CS1}$/CS2</td><td>A0</td><td>D0 ~ D7</td><td>$\overline{RD}$/$\overline{WR}$</td><td>—</td></tr><tr><td>“L”</td><td>$\overline{CS1}$/CS2</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr></table>Note: RAM data read cannot be performed by serial data input. When P/S = L, fix D0 ~ D5 to HZ $\overline{RD}$, and fix $\overline{WR}$ to either “H” or “L”.</td><td>1</td></tr>
</table>

- **LCD Drive Circuit Signals**

Pin	I/O	Function	Number of Pins
M/S	I	This pin selects the master/slave operation of the SED1530 series chips. The master operation outputs the signals necessary for the LCD display. The slave operations input the signals necessary to synchronize the LCD display.	1
CL	I/O	This is the display clock I/O terminal. When using the SED1530 Series chips in master/slave, the CL pins of the chips must be connected. When using in combination with a dedicated common driver, the common driver YSCL pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FR	I/O	This is the LCD alternating current signal I/O pin. When using the SED1530 Series chips in master/slave, the FR pins of the chips must be connected. When using an SED1530 Series chip in master mode, this pin must be connected to the FR pin of the dedicated common driver. M/S = "H": Output M/S = "L": Input	1
DYO	O	This is the common activation output pin. This pin is used only when the SED1530 Series chip is in master mode. This pin must be connected to the common driver DIO pin. This pin is HZ in slave mode.	1
VS1	O	This pin is used to monitor the voltage of the internal power supply.	1
$\overline{DOF}$	I/O	This is the LCD display blanking control pin. When using the SED1530 Series chips in master/slave, the $\overline{DOF}$ pins of the chips must be connected. When using in combination with a dedicated common driver (SED1635), the common driver $\overline{DOFF}$ pin must be connected to this pin. M/S = "H": Output M/S = "L": Input	1
FRS	O	Static drive output pin. This is effective only when in master mode, and is used with the FR pin. This pin is HZ in slave mode.	1

(continued)

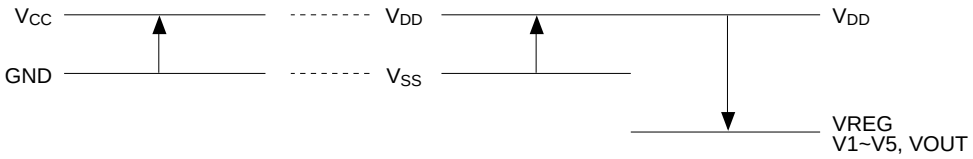
● **LCD Drive Circuit Signals (continued)**

<table>
<tr><th>Pin</th><th>I/O</th><th>Function</th><th>Number of Pins</th></tr>
<tr><td>On
(SEG n)
(COM n)</td><td>O</td><td>LC driver output
This output depends on the model type, as shown below:
<table>
<tr><th></th><th>Segment</th><th>Column</th></tr>
<tr><td>SED1530*0*</td><td>O0 ~ O99</td><td>O100 ~ O131</td></tr>
<tr><td>SED1530*A*</td><td>O16 ~ O115</td><td>O0 ~ O15,
O116 ~ O131</td></tr>
<tr><td>SED1531*0*</td><td>O0 ~ O131</td><td>\</td></tr>
<tr><td>SED1530*0*</td><td>O0 ~ O99</td><td>O100 ~ O131</td></tr>
<tr><td>SED1532*B*</td><td>O32 ~ O131</td><td>O0 ~ O31</td></tr>
</table>
Segment Output Terminal
This is the output for driving the LC segments. Through combining the contents of the display RAM with the FR signal, a single level can be selected from VDD, V2, V3, and V5:
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">On Output Voltage</th></tr>
<tr><th>Positive Display</th><th>Negative Display</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>VDD</td><td>V2</td></tr>
<tr><td>L</td><td>V5</td><td>V3</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V2</td><td>VDD</td></tr>
<tr><td>L</td><td>V3</td><td>V5</td></tr>
<tr><td>Power Save</td><td>—</td><td colspan="2">VDD</td></tr>
</table>
Common Output Terminal
This is the output for driving the LC commons. Through combining the scan data with the FR signal, a single level can be selected from VDD, V1, V4, and V5:
<table>
<tr><th>Scan Data</th><th>FR</th><th>On Output Voltage</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>V5</td></tr>
<tr><td>L</td><td>VDD</td></tr>
<tr><td rowspan="2">L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>V4</td></tr>
<tr><td>Power Save</td><td>—</td><td>VDD</td></tr>
</table></td><td>133</td></tr>
<tr><td>COMS</td><td>O</td><td>This is a common output pin dedicated for the indicator.
Leave open if not used. This pin is functional only for the SED1530 and SED1532. It is HZ for the SED1531.</td><td>1</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Power supply voltage		V_{DD}	–0.3 to +7.0	V
	(at 3× step-up)		–0.3 to +6.0	V
	(at 4× step-up)		–0.3 to +4.5	V
Power supply voltage (2)	(V_{DD} reference)	V5	–18.0 to +0.3	V
Power supply voltage (3)	(V_{DD} reference)	V1, V2, V3, V4	V5 to +0.3	V
Input voltage		V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage		V0	–0.3 to V_{DD} + 0.3	V
Operating temperature		T_{opr}	–30 to +85	°C
Storage temperature	TCP	T_{STR}	–55 to +100	°C
	Bare chip		–55 to +125	°C



Notes:

1. V1 ~ V5, V_{OUT}, and the V5 voltage are all values based on V_{DD} = 0V.
2. The voltages of V1, V2, V3 and V4 must always fulfill the relationship VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5.
3. Permanent damage to the LSI may result if the absolute maximum ratings are exceeded during use. Under normal operation, use should be within the range of the electrical characteristics listed. Violations of these conditions may cause the LSI to malfunction or may cause loss of reliability in the LSI.

● **DC Characteristics**

V_{SS} = 0V, V_{DD} = 5V ±10%, T_a = –40 to 85°C

Parameter			Symbol	Condition		Min	Typ	Max	Unit	Pin
Power supply voltage (1)		Recommended operation	V_{DD}			4.5	5.0	5.5	V	V_{SS} *1
		Possible operation	V_{DD}			2.4	—	6.0		
Operating voltage (2)		Possible operation	V5	V_{DD} reference (V_{DD} = 0V)		–16.0	—	–4.0	V	V5 *2
		Possible operation	V1, V2	V_{DD} reference (V_{DD} = 0V)		0.4 × V5	—	V_{DD}	V	V1, V2
		Possible operation	V3, V4	V_{DD} reference (V_{DD} = 0V)		V5	—	0.6 × V5	V	V3, V4
CMOS	High-level input voltage		V_{IHC}			0.7 × V_{DD}	—	V_{DD}	V	*3
				V_{DD} = 2.7V		0.8 × V_{DD}	—	V_{DD}		
	Low-level input voltage		V_{ILC}			V_{SS}	—	0.3 × V_{DD}	V	*3
				V_{DD} = 2.7V		V_{SS}	—	0.2 × V_{DD}		
	High-level output voltage		V_{OHC}	I_{OH} = 1mA		0.8 × V_{DD}	—	V_{DD}	V	*5
				V_{DD} = 2.7V I_{OH} = –0.5mA		0.8 × V_{DD}	—	V_{DD}		
	Low-level output voltage		V_{OLC}	I_{OL} = 1mA		V_{SS}	—	0.2 × V_{DD}	V	*5
				V_{DD} = 2.7V I_{OL} = 0.5mA		V_{SS}	—	0.2 × V_{DD}		
Schmidt	High-level input voltage		V_{IHS}			0.85 × V_{DD}	—	V_{DD}	V	*4
				V_{DD} = 2.7V		0.8 × V_{DD}	—	V_{DD}		
	Low-level input voltage		V_{ILS}			V_{SS}	—	0.15 × V_{DD}	V	*4
				V_{DD} = 2.7V		V_{SS}	—	0.2 × V_{DD}		
Input leak current			I_{LI}	V_{IN} = V_{DD} or V_{SS}		–1.0	—	1.0	µA	*6
Output leak current			I_{LO}			–3.0	—	3.0	µA	*7
LC driver ON resistance			R_{ON}	T_a = 25°C V_{DD} ref.	V5 = –14.0V	—	2.0	3.0	kΩ	SEG*n*
					V5 = –8.0V	—	3.0	4.5	kΩ	COM*n*
Static consumption current			I_{SSQ}	V_{IN} = V_{DD} or V_{SS}		—	0.01	5.0	µA	V_{SS}
			I_{SQ}	V5 = –18.0V V_{DD} ref.		—	0.01	15.0	µA	V5
Input terminal capacitance			C_{IN}	T_a = 25°C f = 1MHz		—	5.0	8.0	pF	*3, *4
Oscillator frequency			f_{OSC}	T_a = 25°C	V_{DD} = 5.0V	19	22	25	kHz	
					V_{DD} = 2.7V	19	22	25		
Internal Power Supply Circuit	Input voltage		V_{DD}	When 3× step-up		2.4	—	6.0	V	
				When 4× step-up		2.4	—	4.5		
	Booster output voltage		V_{OUT}	When 3× set-up	V_{DD} Ref.	–18.0	—	—	V	V_{OUT}
	Voltage regulator circuit operating voltage		V_{OUT}		V_{DD} Ref.	–18.0	—	–6.0	V	V_{OUT}
	Voltage follower operating voltage		V5 (1)	When applied to the SED1530	V_{DD} Ref.	–16.0	—	–6.0	V	
			V5 (2)	When applied to the SED1531	V_{DD} Ref.	–16.0	—	–4.6	V	
	Reference voltage		V_{REG}	T_a = 25°C	V_{DD} Ref.	–2.65	–2.5	–2.35	V	

- **Dynamic consumption current value (1) in display, internal power supply ON**

Unless otherwise specified, T_a = –40 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1530	I_{DD} (1)	V_{DD} = 5.0V, V5 – V_{DD} = –8.0V, 2× Step-up	—	41	70	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –8.0V, 3× Step-up	—	48	80	µA	
SED1531		V_{DD} = 5.0V, V5 – V_{DD} = –11.0V, 3× Step-up	—	96	160	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –11.0V, 4× Step-up	—	118	190	µA	
SED1532		V_{DD} = 5.0V, V5 – V_{DD} = –11.0V, 3× Step-up	—	96	160	µA	
		V_{DD} = 3.0V, V5 – V_{DD} = –11.0V, 4× Step-up	—	114	190	µA	

- **Current consumption in power save mode**

(V_{SS} = 0V, V_{DD} = 2.7 to 5.5V, T_a = 25°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Standby	I_{DDS1}	SED1530, SED1531, SED1532	—	0.01	1.0	µA
	I_{DDS2}	SED1530, SED1531, SED1532	—	1.0	2.0	µA

Typical current consumption characteristics:

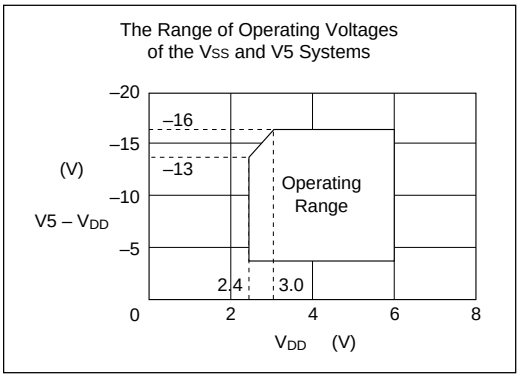
Dynamic current consumption (1)

LCD display status using an external power supply

- **Notes**

*1. Although a broad operating voltage range is guaranteed, this does not guarantee against sudden voltage changes during MPU access.

*2. The range of operating voltages of the V_{DD} system and V5 system. See the figure below. The range of operating voltages applies when the external power supply is used.



*3. The A0, D0 to D5, D6, D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, M/S, C86, P/S and DOF pins.

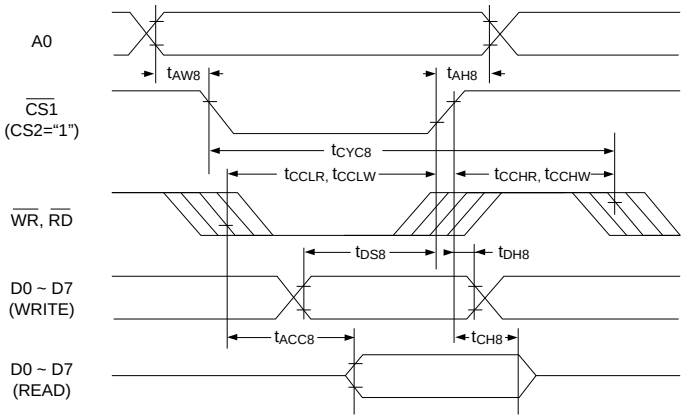
*4. The CL, SCL (D6) and $\overline{RES}$ pins.

*5. The D0 to D5, D6, D7 (SI), FR, FRS, DYO, $\overline{DOF}$ and CL pins.

*6. The A0, $\overline{RD}$, (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, M/S, $\overline{RES}$, C86 and P/S pins.

*7. Applicable when the D0 to D7, FR, CL, DYO and $\overline{DOF}$ pins are in a high impedance state.

- **Timing Characteristics**
  - **System Bus: Read/Write Characteristics I (80-Series MPU)**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		200	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117	—	ns
Data setup time	D0 ~ D7	t_{DS8}		20	—	ns
Data hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	—	70	ns
Output disable time		t_{CH8}		10	50	ns

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

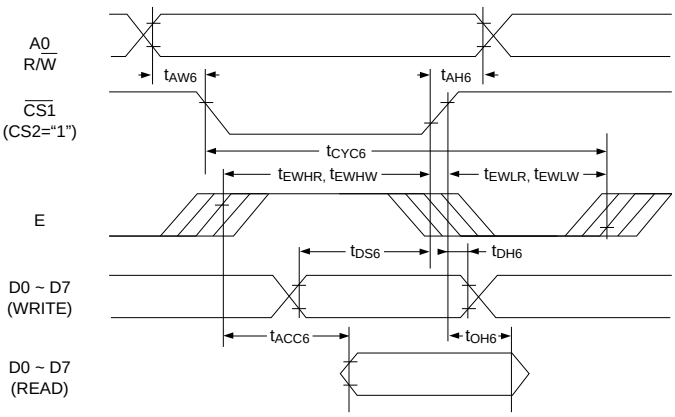
Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Address hold time	A0	t_{AH8}		25	—	ns
Address setup time		t_{AW8}		25	—	ns
System cycle time		t_{CYC8}		450	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244	—	ns
Data setup time	D0 ~ D7	t_{DS8}		40	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL = 100pF	—	140	ns
Output disable time		t_{CH8}		10	100	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less. When the cycle time is used at high speed, the specification is tr + tf ≤ (t_{CYC8} – t_{CCLW} – t_{CCHW}) or tr + tf ≤ (t_{CYC8} – t_{CCLR} – t_{CCHR}).

*2. All timings are specified based on 20% and 80% of V_{DD}.

*3. t_{CCLW} and t_{CCLR} are specified by the overlap period of $\overline{CS1}$ = "0" (CS2 = "1") and $\overline{WR}$, $\overline{RD}$ = "0" level.

○ **System Bus: Read/Write Characteristics I (68-Series MPU)**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time			t_{CYC6}		200	—	ns
Address setup time Address hold time		A0 R/$\overline{W}$	t_{AW6} t_{AH6}		10 10	— —	ns ns
Data setup time Data hold time		D0 ~ D7	t_{DS6} t_{DH6}		20 10	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL = 100pF	10 —	50 70	ns ns
Enable H pulse width	Read	E	t_{EWHR}		77	—	ns
	Write		t_{EWHW}		22	—	ns
Enable L pulse width	Read	E	t_{EWLR}		117	—	ns
	Write		t_{EWLW}		172	—	ns

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

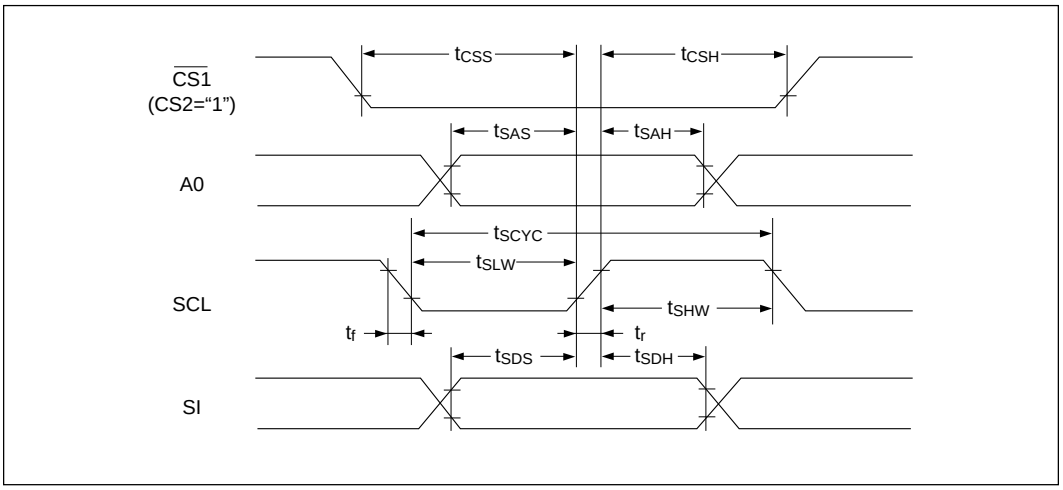
Parameter		Signal	Symbol	Conditions	Min	Max	Unit
System cycle time			t_{CYC6}		450	—	ns
Address setup time Address hold time		A0 R/$\overline{W}$	t_{AW6} t_{AH6}		25 25	— —	ns ns
Data setup time Data hold time		D0 ~ D7	t_{DS6} t_{DH6}		40 20	— —	ns ns
Output disable time Access time			t_{OH6} t_{ACC6}	CL = 100pF	20 —	50 70	ns ns
Enable H pulse width	Read	E	t_{EWHR}		194	—	ns
	Write		t_{EWHW}		44	—	ns
Enable L pulse width	Read	E	t_{EWLR}		244	—	ns
	Write		t_{EWLW}		394	—	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less. When the cycle time is used at high speed, the specification is tr + tf ≤ (t_{CYC8} – t_{EWLW} – t_{EWHW}) or tr + tf ≤ (t_{CYC6} – t_{EWLR} – t_{EWHR}).

*2. All timings are specified based on 20% and 80% of V_{DD}.

*3. t_{EWHR} and t_{EWHW} are specified by the overlap period of $\overline{CS1}$ = "0" (CS2 = "1") and E = "1" level.

○ **Serial Interface**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	t_{SCYC}		500	—	ns
SCL "H" pulse width		t_{SHW}		150	—	ns
SCL "L" pulse width		t_{SLW}		150	—	ns
Address setup time	A0	t_{SAS}		120	—	ns
Address hold time		t_{SAH}		200	—	ns
Data setup time	SI	t_{SDS}		120	—	ns
Data hold time		t_{SDH}		50	—	ns
CS-SCL time	CS	t_{CSS}		30	—	ns
		t_{CSH}		400	—	ns

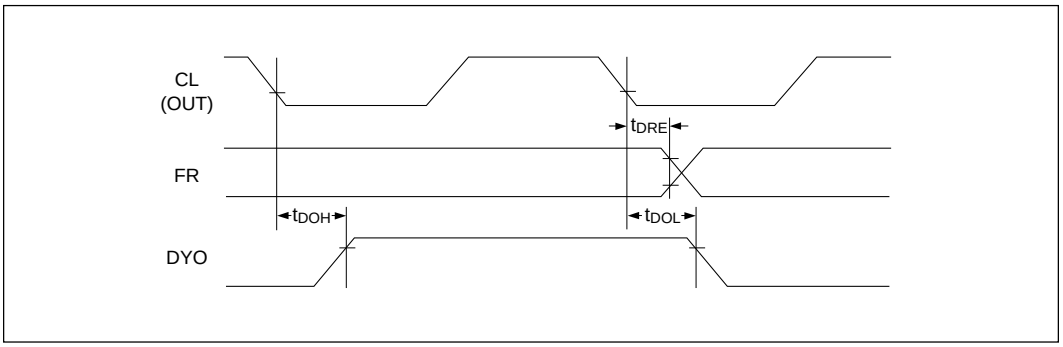
V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Max	Unit
Serial clock period	SCL	t_{SCYC}		1000	—	ns
SCL "H" pulse width		t_{SHW}		300	—	ns
SCL "L" pulse width		t_{SLW}		300	—	ns
Address setup time	A0	t_{SAS}		250	—	ns
Address hold time		t_{SAH}		400	—	ns
Data setup time	SI	t_{SDS}		250	—	ns
Data hold time		t_{SDH}		100	—	ns
CS-SCL time	CS	t_{CSS}		60	—	ns
		t_{CSH}		400	—	ns

*1. The input signal rise time and fall time (tr, tf) are specified at 15ns or less.

*2. All timings are specified based on 20% and 80% of V_{DD}.

○ **Display Control Timing**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 50pF	—	80	150	ns
DYO "H" delay time	DYO	t_{DOH}		—	70	160	ns
DYO "L" delay time		t_{DOL}		—	70	160	ns

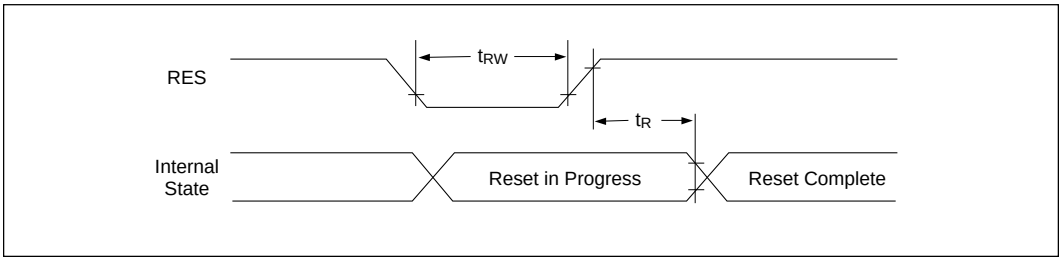
V_{DD} = 2.7 to 4.5V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
FR delay time	FR	t_{DFR}	CL = 50pF	—	120	240	ns
DYO "H" delay time	DYO	t_{DOH}		—	140	250	ns
DYO "L" delay time		t_{DOL}		—	140	250	ns

*1. Effective only when operating in master mode.

*2. All timings are specified based on 20% or 80% of V_{DD}.

○ **Reset Timing**



V_{DD} = 5.0V ± 10%, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		1.0	—	—	ms
Reset "L" pulse width	RES	t_{RW}		1.0	—	—	ms

V_{DD} = 2.7 to 4.5V, T_a = –40 to 85°C

Parameter	Signal	Symbol	Conditions	Min	Typ	Max	Unit
Reset time		t_R		3.0	—	—	ms
Reset "L" pulse width	RES	t_{RW}		3.0	—	—	ms

*1. All timings are specified based on 10% and 90% of V_{DD}.

● **Table of Commands for the SED1530 Series**

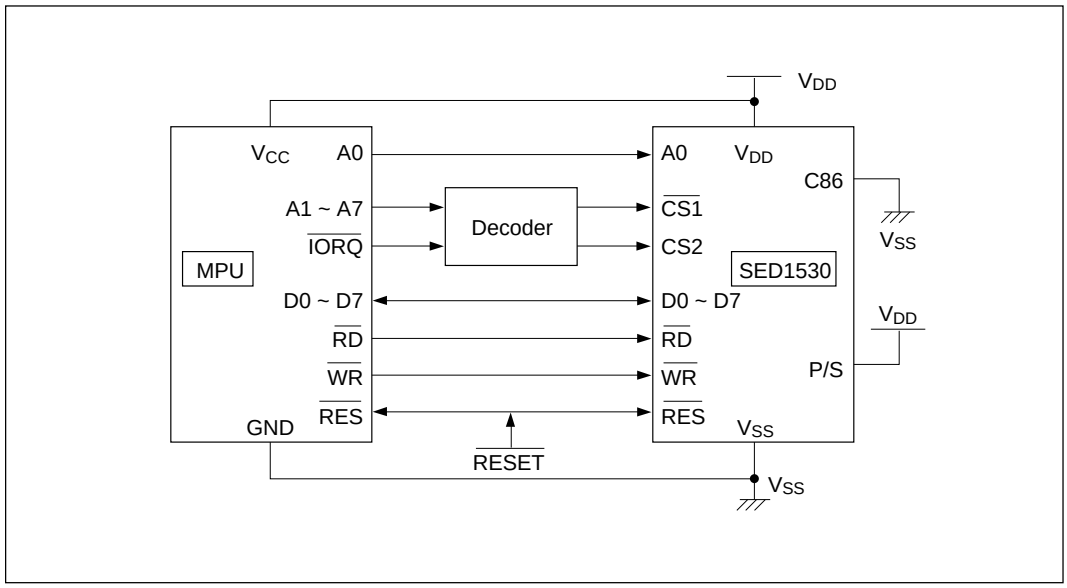
Command		Code											Function
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the LCD display on and off. 0: OFF 1: ON
(2)	Display start line set	0	1	0	0	1	Display start address						Determines the RAM display line displayed to COM0.
(3)	Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page to the page address register.
(4)	Column address set, first 4 bits	0	1	0	0	0	0	1	Most significant column address bits				Sets the 4 most significant bits of the display RAM column address to the register.
(4)	Column address set, last 4 bits	0	1	0	0	0	0	0	Least significant column address bits				Sets the 4 least significant bits of the display RAM column address to the register.
(5)	Status read	0	0	1	Status				0	0	0	0	Read status data.
(6)	Write display data	1	1	0	Write data								Writes to the display RAM.
(7)	Reads display data	1	0	1	Read data								Reads from the display RAM.
(8)	ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the relationship between the display RAM address and the SEG output 0: Normal 1: Reverse
(9)	Display: Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display to normal/ reverse. 0: Normal 1: Reverse
(10)	Display: All Pixel Lit: ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display: All Pixels Lit 0: Normal display 1: All pixels lit
(11)	LCD bias set	0	1	0	1	0	1	0	0	0	1	0	Sets the LCD drive voltage ratio.
(12)	Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address counter by 1 when write, zero when read.
(13)	End	0	1	0	1	1	1	0	1	1	1	0	Gets out of read/modify/write mode.
(14)	Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset.
(15)	Output mode register set	0	1	0	1	1	0	0	0	*	*	*	Selects the direction of the COM output scan. * = disabled
(16)	Power control set	0	1	0	0	0	1	0	1	Operating mode			Selects the power supply circuit operating mode.
(17)	Electronic volume register set	0	1	0	1	0	0	Electronic volume level					Sets the V5 output voltage to the electronic volume register.
(18)	Standby set	0	1	0	1	0	1	0	1	1	0	0 1	Selects the standby mode. 0: OFF 1: ON
(19)	Power save												A composite command with display: OFF and Display: All Pixels On.

Note: Do not use any other command, or a system malfunction may result.

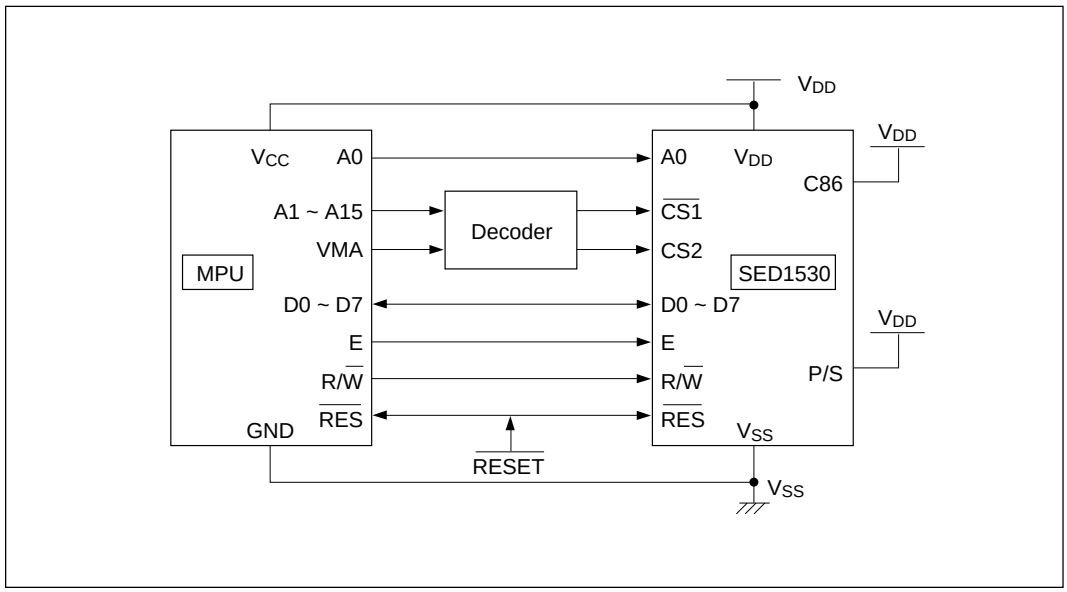
■ MPU INTERFACE (REFERENCE EXAMPLE)

The SED1530 Series chips can be connected to 80-series and 68-series MPUs. Moreover, by utilizing the serial interface, the connections can be made with fewer signal lines. When multiple SED1530 chips are used, each can be connected to the MPU and the chips can be selected using the chip select.

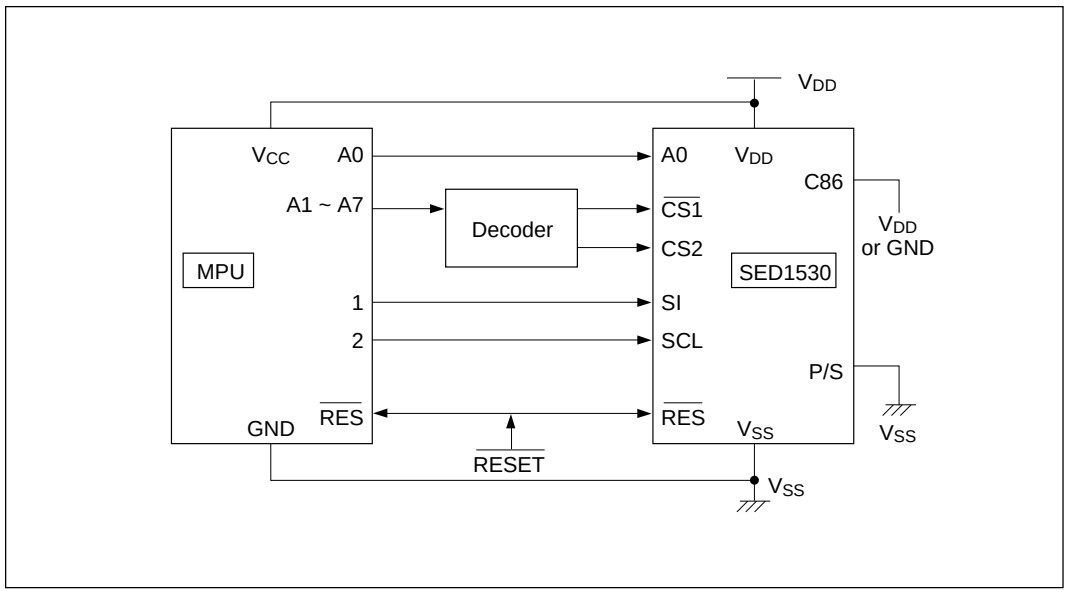
● 80-Series MPU



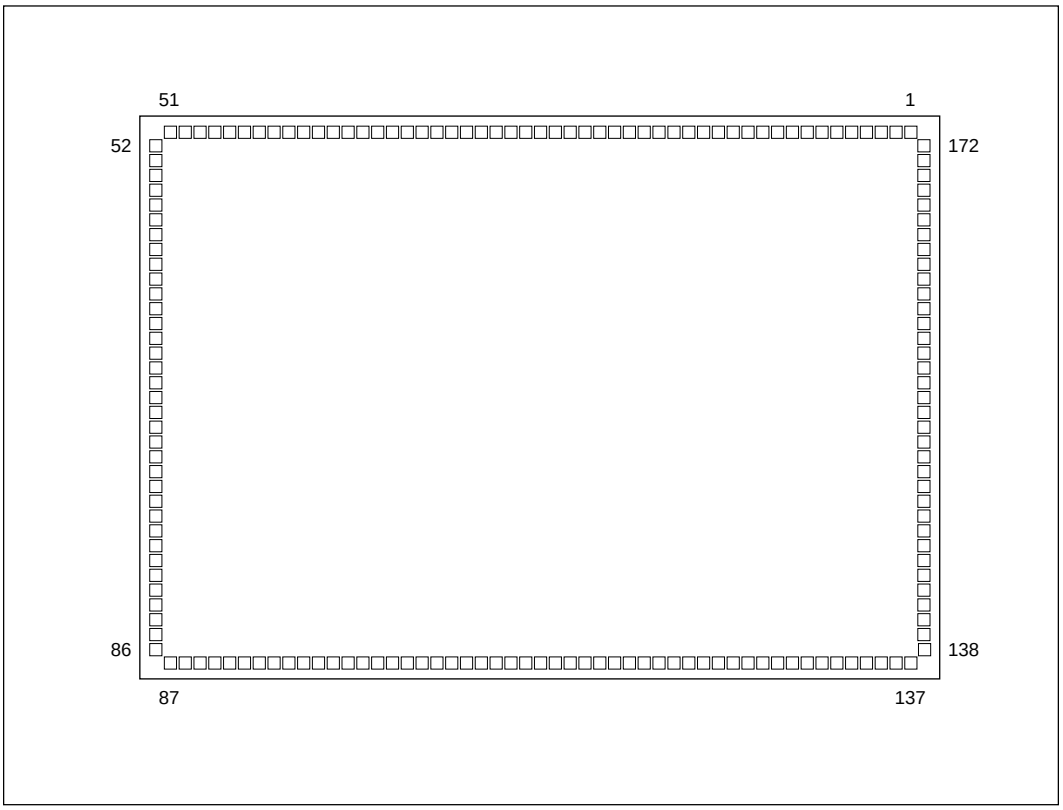
● 68-Series MPU



- **Serial Interface**



■ **PIN LAYOUT**



Chip Size:	6.65 X 4.57 mm
Pad Pitch:	118μm (Min.)
SED153*D*$_{A}$	(Aluminum Pad Model)
Pad Center Size:	90 X 90 μm
Chip Thickness:	300 μm
SED153*D*$_{B}$	(Gold Bump Model)
Bump Size:	76 X 76 μm
Bump Height:	17 to 28 μm (Typ)
Chip Thickness:	625 μm

■ PAD COORDINATES

Unit: μm

No.	Pin Name	X Coord.	Y Coord.
1	O127	2988	2142
2	O128	2860	2142
3	O129	2738	2142
4	O130	2614	2142
5	O131	2490	2142
6	COM3	2386	2142
7	FR5	2242	2142
8	FR	2124	2142
9	DYO	2006	2142
10	CL	1000	2142
11	$\overline{DOF}$	1770	2142
12	VSI	1652	2142
13	M/S	1534	2142
14	$\overline{REG}$	1416	2142
15	P/S	1298	2142
16	$\overline{CS1}$	1180	2142
17	CS2	1062	2142
18	C86	944	2142
19	A0	826	2142
20	$\overline{WR}$ (W/$\overline{R}$)	708	2142
21	$\overline{RD}$ ($\overline{E}$)	590	2142
22	V_{DD}	354	2142
23	D0	236	2142
24	D1	236	2142
25	D2	118	2142
26	D3	0	2142
27	D4	–118	2142
28	D5	–236	2142
29	D6 (SCL)	–354	2142
30	D7 (31)	–472	2142
31	V_{SS}	–590	2142
32	V_{OUT}	–708	2142
33	CAP3–	–826	2142
34	CAP1+	–944	2142
35	CAP1–	–1062	2142
36	CAP2+	–1180	2142
37	CAP2–	–1298	2142
38	V5	–1416	2142
39	VR	–1534	2142
40	V_{DD}	–1652	2142
41	V_1	–1770	2142
42	V_2	–1888	2142
43	V_3	–2006	2142
44	V_4	–2124	2142
45	V_5	–2242	2142
46	O0	–2366	2142
47	O1	–2490	2142
48	O2	–2614	2142
49	O3	–2738	2142
50	O4	–2862	2142
51	O5	–2986	2142
52	O6	–3178	2006
53	O7	–3178	1888
54	O8	–3178	1770
55	O9	–3178	1652
56	O10	–3178	1534
57	O11	–3178	1416
58	O12	–3178	1286
59	O13	–3178	1150
60	O14	–3178	1062
61	O15	–3178	944
62	O16	–3178	826
63	O17	–3178	708
64	O18	–3178	690
65	O19	–3178	472
66	O20	–3178	364
67	O21	–3178	238
68	O22	–3178	118
69	O23	–3178	0
70	O24	–3178	–118
71	O25	–3178	–236
72	O26	–3178	–354
73	O27	–3178	–472
74	O28	–3178	–590
75	O29	–3178	–708
76	O30	–3178	–826
77	O31	–3178	–944
78	O32	–3178	–1062
79	O33	–3178	–1180
80	O34	–3178	–1298
81	O35	–3178	–1418
82	O36	–3178	–1534
83	O37	–3178	–1652
84	O38	–3178	–1770
85	O39	–3178	–1888
86	O40	–3178	–2006
87	O41	–2986	–2142
88	O42	–2862	–2142
89	O43	–2738	–2142
90	O44	–2614	–2142
91	O45	–2490	–2142
92	O46	–2386	–2142
93	O47	–2242	–2142
94	O48	–2124	–2142
95	O49	–2006	–2142
96	O50	–1888	–2142
97	O51	–1770	–2142
98	O52	–1652	–2142
99	O53	–1534	–2142
100	O54	–1416	–2142
101	O55	–1298	–2142
102	O56	–1180	–2142
103	O57	–1062	–2142
104	O58	–944	–2142
105	O59	–826	–2142
106	O60	–708	–2142
107	O61	–590	–2142
108	O62	–472	–2142
109	O63	–354	–2142
110	O64	–236	–2142
111	O65	–118	–2142
112	O66	0	–2142
113	O67	118	–2142
114	O68	236	–2142
115	O69	354	–2142
116	O70	472	–2142
117	O71	590	–2142
118	O72	708	–2142
119	O73	826	–2142
120	O74	944	–2142
121	O75	1062	–2142
122	O76	1180	–2142
123	O77	1298	–2142
124	O78	1416	–2142
125	O79	1534	–2142
126	O80	1652	–2142
127	O81	1770	–2142
128	O82	1888	–2142
129	O83	2006	–2142
130	O84	2124	–2142
131	O85	2242	–2142
132	O86	2366	–2142
133	O87	2490	–2142
134	O88	2614	–2142
135	O89	2738	–2142
136	O90	2862	–2142
137	O91	2986	–2142
138	O92	3178	–2006
139	O93	3178	–1888
140	O94	3178	–1770
141	O95	3178	–1652
142	O96	3178	–1534
143	O97	3178	–1416
144	O98	3178	–1298
145	O99	3178	–1180
146	O100	3178	–1062
147	O101	3178	–944
148	O102	3178	–826
149	O103	3178	–708
150	O104	3178	–590
151	O105	3178	–472
152	O106	3178	–354
153	O107	3178	–236
154	O108	3178	–118
155	O109	3178	0
156	O110	3178	118
157	O111	3178	236
158	O112	3178	354
159	O113	3178	472
160	O114	3178	590
161	O115	3178	708
162	O116	3178	826
163	O117	3178	944
164	O118	3178	1062
165	O119	3178	1180
166	O120	3178	1298
167	O121	3178	1416
168	O122	3178	1534
169	O123	3178	1652
170	O124	3178	1770
171	O125	3178	1888
172	O126	3178	2006

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